

$a_1 >$ 

## 1. Technical Field

2. Related Art

A substrate, such as a chip carrier, typically has a top surface and a bottom surface wherein either surface, or both surfaces, has conductive bonding pads for electrically coupling the substrate to such devices as electronic assemblies (e.g., chips) and electronic carriers (e.g, circuit cards). A conductive bonding pad typically contains copper, but may alternatively contain, inter alia, nickel. Currently, all pads on a given substrate have the same thickness. A reduction in pad thickness generally conserves space on the substrate as a consequence of the outward sloping of pad sidewalls from the top of the pad to the bottom of the pad. The outward sloping is generated by the subtractive etching process used to form the

pads. The outward, or trapezoidal, sloping causes the cross-sectional area of the pad at a pad-substrate interface to decrease with decreasing pad thickness for a given angular slope. The reduction of pad cross-sectional area at the pad-substrate interface allows the pad centers to be more closely spaced, resulting in an overall reduction of the substrate surface area required for implementing the design features of intended applications. The foregoing remarks regarding the use of thin pads to conserve space also apply to circuit lines coupled to the pads inasmuch as the circuit lines may likewise be formed by subtractive etching and consequently have sloping sidewalls. Indeed, a pad may be viewed as volumetric section of a circuit line to which a conductive interconnect, such as a wirebond interconnect or a solder ball, may be electrically and mechanically coupled. Thus, both thin pads and associated thin circuit lines improve space utilization. Pads (and associated circuitizations) may be categorized as to thickness. Such categories include thin pads, thick pads, and medium pads.

A thick pad (and associated circuitization), which typically has a thickness between about 17 microns and about 50 microns, can generally be used for coupling electrical devices and is especially useful for coupling a large solder ball, such as a

solder ball of a ball grid array (BGA), to a substrate for subsequent attachment of the large solder ball to a circuit card.

A thin pad (and associated circuitization), which typically has a thickness between about 3 microns and about 10 microns, can be used for coupling an electronic assembly (e.g., a chip) to a substrate, by use of a wirebond interface (e.g., a gold wire). However, pads are typically made of copper and copper is unsuitable for making a direct attachment of a chip to a substrate by use of a gold wire. To mitigate this problem, the copper pad may be coated with a layer of nickel-gold, wherein a coating of nickel is formed on a top surface of the copper pad, and wherein a coating of gold is formed on the coating of nickel. With the nickel-gold layer over a copper pad, the chip may be wirebonded directly to the gold coating and this wirebond connection is generally reliable. A thin or thick copper pad, with an overlying nickel-gold layer, could also be used for attachment of a BGA solder ball. Note that a thin pad without an overlying nickel-gold layer generally cannot be used for direct attachment of a BGA solder ball, because the soldering process alloys some of the pad metal (e.g., copper) into the bulk of the solder material (e.g., lead/tin). Thus, if the pad is too thin, nearly all of the pad metal may alloy with the solder material,

resulting in an unreliable mechanical and electrical connection.

A medium pad (and associated circuitization) has a thickness between about 10 microns and about 17 microns. A medium pad is particularly useful in flip-chip bonding of a chip to a substrate by use of a small solder ball. Such flip-chip bonding may be accomplished by the controlled collapse chip connection (C4) technique. The diameter of the small solder ball may be nearly an order of magnitude smaller than the diameter of a BGA solder ball (e.g., 2 to 3 mils for a small solder ball versus 25 to 30 mils for a BGA solder ball). The relatively smaller solder ball diameter allows the pad thickness for small solder ball attachment to be less than the pad thickness for BGA solder ball attachment, due to consideration of the alloying of pad metal with the solder material as discussed supra.

It is to be noted that a BGA solder ball can be directly soldered to nickel-gold coating over a thin copper pad, which conserves space. There is controversy, however, as to whether the solder-gold interface is susceptible to joint degradation. Thus, some designers and/or users may prefer to couple a BGA solder ball to a substrate by using a thick, uncoated copper pad than by using a nickel-gold coated thin copper pad. The decision of whether to couple a BGA solder ball to a substrate by using a

thick copper pad or a thin nickel-gold coated copper pad is therefore discretionary and involves balancing the space-saving features of thin pads against reliability concerns associated with thin nickel-gold coated thin copper pads.

5 For applications requiring low-power input to a chip and low processing speed, it may be desirable to have thin circuitization throughout the substrate except where thick BGA pads are required. For applications requiring high-power input to a chip and high processing speed, it may be desirable to have thick circuitization throughout the substrate except where thin wirebond pads are required.

10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26  
27  
28  
29  
30  
31  
32  
33  
34  
35  
36  
37  
38  
39  
40  
41  
42  
43  
44  
45  
46  
47  
48  
49  
50  
51  
52  
53  
54  
55  
56  
57  
58  
59  
60  
61  
62  
63  
64  
65  
66  
67  
68  
69  
70  
71  
72  
73  
74  
75  
76  
77  
78  
79  
80  
81  
82  
83  
84  
85  
86  
87  
88  
89  
90  
91  
92  
93  
94  
95  
96  
97  
98  
99  
100  
101  
102  
103  
104  
105  
106  
107  
108  
109  
110  
111  
112  
113  
114  
115  
116  
117  
118  
119  
120  
121  
122  
123  
124  
125  
126  
127  
128  
129  
130  
131  
132  
133  
134  
135  
136  
137  
138  
139  
140  
141  
142  
143  
144  
145  
146  
147  
148  
149  
150  
151  
152  
153  
154  
155  
156  
157  
158  
159  
160  
161  
162  
163  
164  
165  
166  
167  
168  
169  
170  
171  
172  
173  
174  
175  
176  
177  
178  
179  
180  
181  
182  
183  
184  
185  
186  
187  
188  
189  
190  
191  
192  
193  
194  
195  
196  
197  
198  
199  
200  
201  
202  
203  
204  
205  
206  
207  
208  
209  
210  
211  
212  
213  
214  
215  
216  
217  
218  
219  
220  
221  
222  
223  
224  
225  
226  
227  
228  
229  
230  
231  
232  
233  
234  
235  
236  
237  
238  
239  
240  
241  
242  
243  
244  
245  
246  
247  
248  
249  
250  
251  
252  
253  
254  
255  
256  
257  
258  
259  
260  
261  
262  
263  
264  
265  
266  
267  
268  
269  
270  
271  
272  
273  
274  
275  
276  
277  
278  
279  
280  
281  
282  
283  
284  
285  
286  
287  
288  
289  
290  
291  
292  
293  
294  
295  
296  
297  
298  
299  
300  
301  
302  
303  
304  
305  
306  
307  
308  
309  
310  
311  
312  
313  
314  
315  
316  
317  
318  
319  
320  
321  
322  
323  
324  
325  
326  
327  
328  
329  
330  
331  
332  
333  
334  
335  
336  
337  
338  
339  
340  
341  
342  
343  
344  
345  
346  
347  
348  
349  
350  
351  
352  
353  
354  
355  
356  
357  
358  
359  
360  
361  
362  
363  
364  
365  
366  
367  
368  
369  
370  
371  
372  
373  
374  
375  
376  
377  
378  
379  
380  
381  
382  
383  
384  
385  
386  
387  
388  
389  
390  
391  
392  
393  
394  
395  
396  
397  
398  
399  
400  
401  
402  
403  
404  
405  
406  
407  
408  
409  
410  
411  
412  
413  
414  
415  
416  
417  
418  
419  
420  
421  
422  
423  
424  
425  
426  
427  
428  
429  
430  
431  
432  
433  
434  
435  
436  
437  
438  
439  
440  
441  
442  
443  
444  
445  
446  
447  
448  
449  
450  
451  
452  
453  
454  
455  
456  
457  
458  
459  
460  
461  
462  
463  
464  
465  
466  
467  
468  
469  
470  
471  
472  
473  
474  
475  
476  
477  
478  
479  
480  
481  
482  
483  
484  
485  
486  
487  
488  
489  
490  
491  
492  
493  
494  
495  
496  
497  
498  
499  
500  
501  
502  
503  
504  
505  
506  
507  
508  
509  
510  
511  
512  
513  
514  
515  
516  
517  
518  
519  
520  
521  
522  
523  
524  
525  
526  
527  
528  
529  
530  
531  
532  
533  
534  
535  
536  
537  
538  
539  
540  
541  
542  
543  
544  
545  
546  
547  
548  
549  
550  
551  
552  
553  
554  
555  
556  
557  
558  
559  
560  
561  
562  
563  
564  
565  
566  
567  
568  
569  
570  
571  
572  
573  
574  
575  
576  
577  
578  
579  
580  
581  
582  
583  
584  
585  
586  
587  
588  
589  
590  
591  
592  
593  
594  
595  
596  
597  
598  
599  
600  
601  
602  
603  
604  
605  
606  
607  
608  
609  
610  
611  
612  
613  
614  
615  
616  
617  
618  
619  
620  
621  
622  
623  
624  
625  
626  
627  
628  
629  
630  
631  
632  
633  
634  
635  
636  
637  
638  
639  
640  
641  
642  
643  
644  
645  
646  
647  
648  
649  
650  
651  
652  
653  
654  
655  
656  
657  
658  
659  
660  
661  
662  
663  
664  
665  
666  
667  
668  
669  
670  
671  
672  
673  
674  
675  
676  
677  
678  
679  
680  
681  
682  
683  
684  
685  
686  
687  
688  
689  
690  
691  
692  
693  
694  
695  
696  
697  
698  
699  
700  
701  
702  
703  
704  
705  
706  
707  
708  
709  
710  
711  
712  
713  
714  
715  
716  
717  
718  
719  
720  
721  
722  
723  
724  
725  
726  
727  
728  
729  
730  
731  
732  
733  
734  
735  
736  
737  
738  
739  
740  
741  
742  
743  
744  
745  
746  
747  
748  
749  
750  
751  
752  
753  
754  
755  
756  
757  
758  
759  
760  
761  
762  
763  
764  
765  
766  
767  
768  
769  
770  
771  
772  
773  
774  
775  
776  
777  
778  
779  
780  
781  
782  
783  
784  
785  
786  
787  
788  
789  
790  
791  
792  
793  
794  
795  
796  
797  
798  
799  
800  
801  
802  
803  
804  
805  
806  
807  
808  
809  
810  
811  
812  
813  
814  
815  
816  
817  
818  
819  
820  
821  
822  
823  
824  
825  
826  
827  
828  
829  
830  
831  
832  
833  
834  
835  
836  
837  
838  
839  
840  
841  
842  
843  
844  
845  
846  
847  
848  
849  
850  
851  
852  
853  
854  
855  
856  
857  
858  
859  
860  
861  
862  
863  
864  
865  
866  
867  
868  
869  
870  
871  
872  
873  
874  
875  
876  
877  
878  
879  
880  
881  
882  
883  
884  
885  
886  
887  
888  
889  
890  
891  
892  
893  
894  
895  
896  
897  
898  
899  
900  
901  
902  
903  
904  
905  
906  
907  
908  
909  
910  
911  
912  
913  
914  
915  
916  
917  
918  
919  
920  
921  
922  
923  
924  
925  
926  
927  
928  
929  
930  
931  
932  
933  
934  
935  
936  
937  
938  
939  
940  
941  
942  
943  
944  
945  
946  
947  
948  
949  
950  
951  
952  
953  
954  
955  
956  
957  
958  
959  
960  
961  
962  
963  
964  
965  
966  
967  
968  
969  
970  
971  
972  
973  
974  
975  
976  
977  
978  
979  
980  
981  
982  
983  
984  
985  
986  
987  
988  
989  
990  
991  
992  
993  
994  
995  
996  
997  
998  
999  
1000  
1001  
1002  
1003  
1004  
1005  
1006  
1007  
1008  
1009  
1010  
1011  
1012  
1013  
1014  
1015  
1016  
1017  
1018  
1019  
1020  
1021  
1022  
1023  
1024  
1025  
1026  
1027  
1028  
1029  
1030  
1031  
1032  
1033  
1034  
1035  
1036  
1037  
1038  
1039  
1040  
1041  
1042  
1043  
1044  
1045  
1046  
1047  
1048  
1049  
1050  
1051  
1052  
1053  
1054  
1055  
1056  
1057  
1058  
1059  
1060  
1061  
1062  
1063  
1064  
1065  
1066  
1067  
1068  
1069  
1070  
1071  
1072  
1073  
1074  
1075  
1076  
1077  
1078  
1079  
1080  
1081  
1082  
1083  
1084  
1085  
1086  
1087  
1088  
1089  
1090  
1091  
1092  
1093  
1094  
1095  
1096  
1097  
1098  
1099  
1100  
1101  
1102  
1103  
1104  
1105  
1106  
1107  
1108  
1109  
1110  
1111  
1112  
1113  
1114  
1115  
1116  
1117  
1118  
1119  
1120  
1121  
1122  
1123  
1124  
1125  
1126  
1127  
1128  
1129  
1130  
1131  
1132  
1133  
1134  
1135  
1136  
1137  
1138  
1139  
1140  
1141  
1142  
1143  
1144  
1145  
1146  
1147  
1148  
1149  
1150  
1151  
1152  
1153  
1154  
1155  
1156  
1157  
1158  
1159  
1160  
1161  
1162  
1163  
1164  
1165  
1166  
1167  
1168  
1169  
1170  
1171  
1172  
1173  
1174  
1175  
1176  
1177  
1178  
1179  
1180  
1181  
1182  
1183  
1184  
1185  
1186  
1187  
1188  
1189  
1190  
1191  
1192  
1193  
1194  
1195  
1196  
1197  
1198  
1199  
1200  
1201  
1202  
1203  
1204  
1205  
1206  
1207  
1208  
1209  
1210  
1211  
1212  
1213  
1214  
1215  
1216  
1217  
1218  
1219  
1220  
1221  
1222  
1223  
1224  
1225  
1226  
1227  
1228  
1229  
1230  
1231  
1232  
1233  
1234  
1235  
1236  
1237  
1238  
1239  
1240  
1241  
1242  
1243  
1244  
1245  
1246  
1247  
1248  
1249  
1250  
1251  
1252  
1253  
1254  
1255  
1256  
1257  
1258  
1259  
1260  
1261  
1262  
1263  
1264  
1265  
1266  
1267  
1268  
1269  
1270  
1271  
1272  
1273  
1274  
1275  
1276  
1277  
1278  
1279  
1280  
1281  
1282  
1283  
1284  
1285  
1286  
1287  
1288  
1289  
1290  
1291  
1292  
1293  
1294  
1295  
1296  
1297  
1298  
1299  
1300  
1301  
1302  
1303  
1304  
1305  
1306  
1307  
1308  
1309  
1310  
1311  
1312  
1313  
1314  
1315  
1316  
1317  
1318  
1319  
1320  
1321  
1322  
1323  
1324  
1325  
1326  
1327  
1328  
1329  
1330  
1331  
1332  
1333  
1334  
1335  
1336  
1337  
1338  
1339  
1340  
1341  
1342  
1343  
1344  
1345  
1346  
1347  
1348  
1349  
1350  
1351  
1352  
1353  
1354  
1355  
1356  
1357  
1358  
1359  
1360  
1361  
1362  
1363  
1364  
1365  
1366  
1367  
1368  
1369  
1370  
1371  
1372  
1373  
1374  
1375  
1376  
1377  
1378  
1379  
1380  
1381  
1382  
1383  
1384  
1385  
1386  
1387  
1388  
1389  
1390  
1391  
1392  
1393  
1394  
1395  
1396  
1397  
1398  
1399  
1400  
1401  
1402  
1403  
1404  
1405  
1406  
1407  
1408  
1409  
1410  
1411  
1412  
1413  
1414  
1415  
1416  
1417  
1418  
1419  
1420  
1421  
1422  
1423  
1424  
1425  
1426  
1427  
1428  
1429  
1430  
1431  
1432  
1433  
1434  
1435  
1436  
1437  
1438  
1439  
1440  
1441  
1442  
1443  
1444  
1445  
1446  
1447  
1448  
1449  
1450  
1451  
1452  
1453  
1454  
1455  
1456  
1457  
1458  
1459  
1460  
1461  
1462  
1463  
1464  
1465  
1466  
1467  
1468  
1469  
1470  
1471  
1472  
1473  
1474  
1475  
1476  
1477  
1478  
1479  
1480  
1481  
1482  
1483  
1484  
1485  
1486  
1487  
1488  
1489  
1490  
1491  
1492  
1493  
1494  
1495  
1496  
1497  
1498  
1499  
1500  
1501  
1502  
1503  
1504  
1505  
1506  
1507  
1508  
1509  
1510  
1511  
1512  
1513  
1514  
1515  
1516  
1517  
1518  
1519  
1520  
1521  
1522  
1523  
1524  
1525  
1526  
1527  
1528  
1529  
1530  
1531  
1532  
1533  
1534  
1535  
1536  
1537  
1538  
1539  
1540  
1541  
1542  
1543  
1544  
1545  
1546  
1547  
1548  
1549  
1550  
1551  
1552  
1553  
1554  
1555  
1556  
1557  
1558  
1559  
1560  
1561  
1562  
1563  
1564  
1565  
1566  
1567  
1568  
1569  
1570  
1571  
1572  
1573  
1574  
1575  
1576  
1577  
1578  
1579  
1580  
1581  
1582  
1583  
1584  
1585  
1586  
1587  
1588  
1589  
1590  
1591  
1592  
1593  
1594  
1595  
1596  
1597  
1598  
1599  
1600  
1601  
1602  
1603  
1604  
1605  
1606  
1607  
1608  
1609  
1610  
1611  
1612  
1613  
1614  
1615  
1616  
1617  
1618  
1619  
1620  
1621  
1622  
1623  
1624  
1625  
1626  
1627  
1628  
1629  
1630  
1631  
1632  
1633  
1634  
1635  
1636  
1637  
1638  
1639  
1640  
1641  
1642  
1643  
1644  
1645  
1646  
1647  
1648  
1649  
1650  
1651  
1652  
1653  
1654  
1655  
1656  
1657  
1658  
1659  
1660  
1661  
1662  
1663  
1664  
1665  
1666  
1667  
1668  
1669  
1670  
1671  
1672  
1673  
1674  
1675  
1676  
1677  
1678  
1679  
1680  
1681  
1682  
1683  
1684  
1685  
1686  
1687  
1688  
1689  
1690  
1691  
1692  
1693  
1694  
1695  
1696  
1697  
1698  
1699  
1700  
1701  
1702  
1703  
1704  
1705  
1706  
1707  
1708  
1709  
1710  
1711  
1712  
1713  
1714  
1715  
1716  
1717  
1718  
1719  
1720  
1721  
1722  
1723  
1724  
1725  
1726  
1727  
1728  
1729  
1730  
1731  
1732  
1733  
1734  
1735  
1736  
1737  
1738  
1739  
1740  
1741  
1742  
1743  
1744  
1745  
1746  
1747  
1748  
1749  
1750  
1751  
1752  
1753  
1754  
1755  
1756  
1757  
1758  
1759  
1760  
1761  
1762  
1763  
1764  
1765  
1766  
1767  
1768  
1769  
1770  
1771  
1772  
1773  
1774  
1775  
1776  
1777  
1778  
1779  
1780  
1781  
1782  
1783  
1784  
1785  
1786  
1787  
1788  
1789  
1790  
1791  
1792  
1793  
1794  
1795  
1796  
1797  
1798  
1799  
1800  
1801  
1802  
1803  
1804  
1805  
1806  
1807  
1808  
1809  
1810  
1811  
1812  
1813  
1814  
1815  
1816  
1817  
1818  
1819  
1820  
1821  
1822  
1823  
1824  
1825  
1826  
1827  
1828  
1829  
1830  
1831  
1832  
1833  
1834  
1835  
1836  
1837  
1838  
1839  
1840  
1841  
1842  
1843  
1844  
1845  
1846  
1847  
1848  
1849  
1850  
1851  
1852  
1853  
1854  
1855  
1856  
1857  
1858  
1859  
1860  
1861  
1862  
1863  
1864  
1865  
1866  
1867  
1868  
1869  
1870  
1871  
1872  
1873  
1874  
1875  
1876  
1877  
1878  
1879  
1880  
1881  
1882  
1883  
1884  
1885  
1886  
1887  
1888  
1889  
1890  
1891  
1892  
1893  
1894  
1895  
1896  
1897  
1898  
1899  
1900  
1901  
1902  
1903  
1904  
1905  
1906  
1907  
1908  
1909  
1910  
1911  
1912  
1913  
1914  
1915  
1916  
1917  
1918  
1919  
1920  
1921  
1922  
1923  
1924  
1925  
1926  
1927  
1928  
1929  
1930  
1931  
1932  
1933  
1934  
1935  
1936  
1937  
1938  
1939  
1940  
1941  
1942  
1943  
1944  
1945  
1946  
1947  
1948  
1949  
1950  
1951  
1952  
1953  
1954  
1955  
1956  
1957  
1958  
1959  
1960  
1961  
1962  
1963  
1964  
1965  
1966  
1967  
1968  
1969  
1970  
1971  
1972  
1973  
1974  
1975  
1976  
1977  
1978  
1979  
1980  
1981  
1982  
1983  
1984  
1985  
1986  
1987  
1988  
1989  
1990  
1991  
1992  
1993  
1994  
1995  
1996  
1997  
1998  
1999  
2000  
2001  
2002  
2003  
2004  
2005  
2006  
2007  
2008  
2009  
2010  
2011  
2012  
2013  
2014  
2015  
2016  
2017  
2018  
2019  
2020  
2021  
2022  
2023  
2024  
2025  
2026  
2027  
2028  
2029  
2030  
2031  
2032  
2033  
2034  
2035  
2036  
2037  
2038  
2039  
2040  
2041  
2042  
2043  
2044  
2045  
2046  
2047  
2048  
2049  
2050  
2051  
2052  
2053  
2054  
2055  
2056  
2057  
2058  
2059  
2060  
2061  
2062  
2063  
2064  
2065  
2066  
2067  
2068  
2069  
2070  
2071  
2072  
2073  
2074  
2075  
2076  
2077  
2078  
2079  
2080  
2081  
2082  
2083  
2084  
2085  
2086  
2087  
2088  
2089  
2090  
2091  
2092  
2093  
2094  
2095  
2096  
2097  
2098  
2099  
2100  
2101  
2102  
2103  
2104  
2105  
2106  
2107  
2108  
2109  
2110  
2111  
2112  
2113  
2114  
2115  
2116  
2117  
2118  
2119  
2120  
2121  
2122  
2123  
2124  
2125  
2126  
2127  
2128  
2129  
2130  
2131  
2132  
2133  
2134  
2135  
2136  
2137  
2138  
2139  
2140  
2141  
2142  
2143  
2144  
2145  
2146  
2147  
2148  
2149  
2150  
2151  
2152  
2153  
2154  
2155  
2156  
2157  
2158  
2159  
2160  
2161  
2162  
2163  
2164  
2165  
2166  
2167  
2168  
2169  
2170  
2171  
2172  
2173  
2174  
2175  
2176  
2177  
2178  
2179  
2180  
2181  
2182  
2183  
2184  
2185  
2186  
2187  
2188  
2189  
2190  
2191  
2192  
2193  
2194  
2195  
2196  
2197  
2198  
2199  
2200  
2201  
2202  
2203  
2204  
2205  
2206  
2207  
2208  
2209  
2210  
2211  
2212  
2213  
2214  
2215  
2216  
2217  
2218  
2219  
22

a first circuit line including a first conductive pad and having a first thickness, wherein the first circuit line is coupled to the substrate; and

5 a second circuit line including a second conductive pad and having a second thickness that is unequal to the first thickness, wherein the second circuit line is coupled to the substrate, and wherein the second circuit line is electrically coupled to the first circuit line.

The present invention also provides a method for forming an electronic structure, comprising:

providing a substrate;

forming a first circuit line that includes a first conductive pad and has a first thickness;

coupling the first circuit line to the substrate;

forming a second circuit line that includes a second conductive pad and has a second thickness that is unequal to the first thickness;

coupling the second circuit line to the substrate; and

20 electrically coupling the second circuit line to the first circuit line.

The present invention has the advantage of allowing pads and associated circuit lines on the same substrate to have different

thicknesses, which enables the benefits associated with each circuit line thickness and each pad thickness to be realized.

The present invention has the advantage of allowing thick BGA pads and thin wirebond pads to exist on the same substrate.

5 The present invention has the advantage of allowing thick BGA pads and medium C4 solder-ball pads to exist on the same substrate.

The present invention has the advantage of allowing thin wirebond pads and medium C4 solder-ball pads to exist on the same substrate.

10 The present invention has the advantage of allowing applications requiring low-power input to a chip and low processing speed to have thin circuitization throughout the substrate except where thick BGA pads are required.

The present invention has the advantage of applications requiring high-power input to a chip and high processing speed to have thick circuitization throughout the substrate except where thin wirebond pads are required.

#### Brief Description of the Drawings

20 FIG. 1 depicts a front cross-sectional view of a substrate with a plated through hole (PTH) and added metal foil layers, in

accordance with an initial step of a preferred embodiment of the process of the present invention.

FIG. 2 depicts FIG. 1 with indicated regions to be circuitized to thicknesses of the metal foil layers.

5 FIG. 3 depicts FIG. 2 after the indicated regions have been circuitized to form first, second, and third circuit lines.

FIG. 4 depicts a top perspective view of the configuration of FIG. 3.

FIG. 5 depicts FIG. 3 after metallic coatings have been formed on a surface of the first circuit line.

10 FIG. 6 depicts FIG. 5 after metal has been plated on the metal foil to form metal layers.

FIG. 7 depicts FIG. 6 with indicated regions to be circuitized to thicknesses of the metal layers.

15 FIG. 8 depicts FIG. 7 after the indicated regions have been circuitized to form fourth, fifth, and sixth circuit lines.

FIG. 9 depicts a top view of a first preferred embodiment of the structure of the present invention.

20 FIG. 10 depicts a front cross-sectional view of a second preferred embodiment of the structure of the present invention.

FIG. 11 depicts a front cross-sectional view of a third preferred embodiment of the structure of the present invention.

FIG. 12 depicts a front cross-sectional view of a fourth preferred embodiment of the structure of the present invention.

#### Detailed Description of the Invention

FIGS. 1-8 illustrate a preferred embodiment of the method of the present invention. FIG. 1 illustrates a front cross-sectional view of a substrate 10 with a plated through hole (PTH) 12, a top layer of metal foil 14 on the top surface 18 of the substrate 10, and a bottom layer of metal foil 16 on the bottom surface 19 of the substrate 10. The substrate 10 may represent a device such as a chip carrier. The PTH 12 has a plated metal inner wall 13 for providing conductive coupling between circuitizations to be subsequently formed on both the top surface 18 and the bottom surface 19. The PTH may be filled with an insulative material to prevent seepage of matter into the PTH during subsequent fabrication steps. The top layer of metal foil 14 on the top surface 18, having a thickness  $t_1$ , may be formed by any known method. It is common to first form a metal foil of standard thickness exceeding  $t_1$  on the top surface 18, followed by chemically etching the metal foil down to the thickness  $t_1$ . The thickness  $t_2$  of the bottom layer of metal foil 16 may be formed by any known method, including a method similar to that

used for forming the thickness  $t_1$  of the top layer of metal foil 14. Note that  $t_2$  may be unequal to  $t_1$ . The material of the top layer metal foil 14, and of the bottom layer of metal foil 16, may be any material that could be used for forming conductive pads and associated circuit lines. A conductive pad typically contains copper, but may alternatively contain, inter alia, nickel.

FIG. 2 illustrates FIG. 1 after identification of regions to be subsequently circuitized, namely regions 20 and 22 within the top layer of metal foil 14, and region 24 within the bottom layer of metal foil 16. FIG. 3 illustrates FIG. 2 after formation of a first circuit line 30 of thickness  $t_1$ , a second circuit line 32 of thickness  $t_1$ , and a third circuit line 34 of thickness  $t_2$ , from regions 20, 22, and 24 (see FIG. 2 for regions 20, 22, and 24), respectively. The first circuit line 30, second circuit line 32, and third circuit line 34 in FIG. 3 may be formed by any method known in the art, such as by photolithography with subtractive etching. Employing photolithography includes applying, exposing, developing, etching, and stripping steps. In the applying step, photoresist is applied to the open surfaces of the metal foil layers 14 and 16 in FIG. 2. An open surface is defined as a surface that is open to (i.e., in contact with) the

atmosphere. In the exposing step, the photoresist-covered surfaces under which circuitizations will be subsequently formed are selectively exposed to light of a suitable wavelength (e.g., ultraviolet light). With particular reference to FIG. 2, the light is selectively directed to surfaces under which the first circuit line 30, the second circuit line 32, and the third circuit line 34 will be subsequently formed; i.e., to the surface 35 of region 20, the surface 37 of region 22, and the surface 38 of region 24. The light is also directed to surfaces under which additional circuitizations will be subsequently formed as will be described *infra*, namely the open surfaces 44 of the top layer of metal foil 14 and the open surfaces 46 of the bottom layer of metal foil 14, as shown in FIG. 2 and FIG. 3. The photoresist that is exposed to the selectively directed light is protected in the subsequent developing step. In the developing step, the photoresist is developed away from surfaces not previously exposed (said surfaces not shown in FIG. 3). In the etching step, the unprotected metal (i.e., unexposed metal) of the metal foil layers 14 and 16 is removed by chemical etching, resulting in the formation of circuit lines 30, 32, and 34 shown in FIG. 3. The removal of the unprotected metal generates void space adjacent to circuit lines 30, 32, and 34. This void space is not

depicted in FIG. 3, because the cross-sectional view of FIG. 3 does not traverse the void space. The projected widths  $w_1$  and  $w_2$  of the first circuit line 30 and the second circuit line 32, respectively, serve to correlate the top view of FIG. 4 with the cross-sectional view of FIG. 3. After the etching step, some metal foil 14 and some metal foil 16 remains, namely the metal foil 14 having open surfaces 44, and the metal foil 16 having open surfaces 46. In the stripping step, the exposed photoresist is stripped away.

FIG. 4 illustrates of top view of the configuration of FIG. 3, showing the top layer of metal foil 14 and not showing the bottom layer of metal foil 16. The aforementioned subtractive etching process (described *supra* in conjunction with FIG. 3) generates a first void space 31 surrounding the first circuit line 30, and a second void space 33 surrounding the second circuit line 32, as shown in FIG. 4. The first void space 31 and the second void space 33 define the geometric features of the first circuit line 30 and the second circuit line 32, respectively. The projected widths  $w_1$  and  $w_2$  of the first circuit line 30 and the second circuit line 32, respectively, serve to correlate the top view of FIG. 4 with the front view of FIG. 3. Although FIG. 4 does not show the third circuit line 34

of FIG. 3, it should be noted that there is void space around the third circuit line 34 that defines the geometric features of third circuit line 34. While the first circuit line 30 is only one circuit line within the first void space 31, as illustrated in FIG. 4, the process of the present invention could generate a plurality of circuit lines within the first void space 31 such that void space exists between each pair of adjacent circuit lines. Similarly, the second void space 33 could include a plurality of circuit lines. It should be noted that a circuit line, such as the first circuit line 30 or the second circuit line 32, may include a designated volumetric section (i.e., a "pad") for subsequent coupling with an electrical connector, such as a wirebond connector or a solder ball. A "pad" is defined as a volumetric section of a circuit line to which a conductive interconnect, such as a wirebond interconnect or a solder ball, may be electrically and mechanically coupled.

FIG. 5 illustrates FIG. 3 after a metallic coating 40 is formed by any known method, such as plating (e.g., electroplating), on a portion 36 of the open surface 35 of the first circuit line 30. The metallic coating 40 may serve to conductively couple a wirebond interface, such as a gold wire, to the portion 36. The metallic coating 40 may be formed by any

method known by one skilled in the art. A known method involves photolithographic steps comprising applying, exposing, developing, plating, and stripping steps. In the applying step, photoresist is applied to all currently open surfaces 44 of the first metal foil layer 14, the open surfaces 46 of the second metal foil layer 16, the open surface 35 of the first circuit line 30, the open surface 37 of the second circuit line 32, and the open surface 38 of the third circuit line 34. The purpose of applying photoresist to all open surfaces is to protect all open surfaces from being plated in the subsequent plating step, except those open surfaces which are exposed in the subsequent exposing step that precedes the plating step. Next, in the exposing step, light of a suitable wavelength (e.g., ultraviolet light) is selectively directed to portions of the photoresist-covered surfaces which will not be subsequently plated by the metallic coating 40. In particular, light of the wavelength will not be directed to the portion 36 of the open surface 35 of the first circuit line 30. The photoresist that is exposed to the selectively directed light is protected in the subsequent developing step. In the developing step, the photoresist is developed away from surfaces not previously exposed to light, namely the portion 3 (i.e., the copper in the first circuit line

30). In the plating step, the metallic coating 40 is plated on the portion 36. In the stripping step, the exposed photoresist is stripped away. For some applications, the metallic coating 40 includes a first metallic coating 41 plated on the portion 36, and a second metallic coating 42 plated on the first metallic coating 41. For example, a wirebond interface of a gold wire cannot directly bond with the first circuit line 30 made of copper. To solve this particular problem, the metallic coating 40 includes a first metallic coating 41 made of nickel, and second metallic coating 42 made of gold. The second metallic coating 42 could alternatively be made of, inter alia, palladium. The nickel in the first metallic coating 41 acts as a diffusion barrier to prevent gold from diffusing into the copper material located underneath the portion 36. The first metallic coating 41 should be at least about 2.5 microns thick in order to effectively serve as a diffusion barrier and also to reliably maintain its structural integrity. The second metallic coating 42 should be at least about 0.5 microns thick in order to be reliably bond with a wirebond interface.

FIG. 6 depicts FIG. 5 after the layer of metal foil 14 (see FIG. 5) is transformed into a top metal layer 50 of thickness  $t_2$  that exceeds  $t_1$ , and after the layer of metal foil 16 (see FIG.

5) is transformed into a top metal layer 54 of thickness  $t_4$  that exceeds  $t_2$ . Returning to FIG. 5, the aforementioned transformations are accomplished in several steps. First, all open surfaces (44, 35, 40, 37, 46, and 38) are covered with photoresist. Second, all photoresist-covered surfaces, except surfaces 44 and 46, are protectively exposed to light of a suitable wavelength such as ultraviolet light. Third, the unexposed photoresist on surfaces 44 and 46 is developed away. Fourth, the same metal as is in the top layer of metal foil 14 is plated on the open surfaces 44 to form, together with underneath top layer metal foil 14, the top metal layer 50 shown in FIG. 6. Similarly, the same metal as is in the bottom layer of metal foil 16 is plated on the open surfaces 46 to form, together with underneath bottom layer metal foil 16, the bottom metal layer 54. The remaining exposed surfaces are protected from being plated.

FIG. 7 illustrates FIG. 6 after identification of regions to be subsequently circuitized, namely region 56 within the top metal layer 50, and regions 58 and 60 within the bottom metal layer 54. FIG. 8 illustrates FIG. 7 after formation of a fourth circuit line 70 of thickness  $t_3$ , a fifth circuit line 72 of thickness  $t_4$ , and a sixth circuit line 74 of thickness  $t_4$ , from regions 56, 58, and 60 (see FIG. 7 for regions 56, 58, and 60),

respectively. The fourth circuit line 70, fifth circuit line 72, and sixth circuit line 74 in FIG. 8 may be formed by any method known in the art, such as by subtractive etching. With subtractive etching in consideration of the existing exposed photoresist (discussed *supra* in connection with FIG. 6), the unprotected metal (i.e., unexposed metal) of the top metal layer 50, as well as the unprotected metal of the bottom metal layer 54, is removed by chemical etching so as to form the fourth circuit line 70, the fifth circuit line 72, and the sixth circuit line 74. Next, the exposed photoresist is stripped away. It should be noted that any volumetric portion of circuit lines 70, 72, and 74 may constitute a "pad" for subsequent coupling with an electrical connector, such as a wirebond interconnect or a solder ball.

The preceding steps, resulting in the electronic structure illustrated in FIG. 8, for forming the top metal layer 50 and the bottom metal layer 54 and subsequently forming circuit lines 70, 72, and 74, may be repeated to form additional circuitization layers. In particular, the relevant steps (applying photoresist, selectively exposing the photoresist, developing away unexposed photoresist, plating metal on unexposed surfaces, and subtractive etching to define circuit line geometric features) may be used to

form a top circuitization layer of thickness  $t_3$ , (exceeding  $t_3$ ) on the top surface 18 of the substrate 10, and a circuitization layer of thickness  $t_4$ , (exceeding  $t_4$ ) on the bottom surface 19 of the substrate 10. In this manner an arbitrary finite number of circuitization layers may be generated on a substrate by the method of the present invention. Each formed circuitization layer has a greater thickness than the prior formed circuitization layers on the same surface (top surface 18 or bottom surface 19) of the substrate 10.

After all circuitization layers have been formed, a portion of any circuitization layer may be covered by a protective coating. Such coatings may include, inter alia, an organic photoresist, a polyimide, an acrylic, or an epoxy. As an example, the protective coating 78 in FIG. 8 covers a portion of the fifth circuit line 72 and the second circuit line 34.

*C2* Any two circuit lines of different thickness may be formed to be conductively coupled such that a pad on one of the two circuit lines couples the substrate to an electronic assembly, such as a chip, and the other of the two circuit lines couples the substrate to an electronic carrier, such as a circuit card. See, e.g, FIGS. 10-12, to be discussed *infra*, for various illustrative electrical structures of the present invention.

FIG. 8 illustrates that first circuit line 30 may be conductively coupled with fourth circuit line 70, and third circuit line 34 may be conductively coupled with fifth circuit line 72, which illustrate the electrical coupling of two circuit lines of different thickness located on the same surface of a substrate. The second circuit line 32 may be conductively coupled with sixth circuit line 74 by use of the PTH 12, thereby electrically coupling two circuit lines of different thickness located on opposite surfaces of a substrate. Any known variation of the electrical structure illustrated by the PTH 12 may be used to electrically couple two circuit lines of different thickness located on opposite surfaces of a substrate. For example, the second circuit line 32 may be electrically coupled to a first PTH, the sixth circuit line 74 may be electrically coupled to a second PTH, and the first PTH may be electrically coupled to the second PTH by a conductive plane within the substrate or by a plurality of electrically coupled conductive planes within the substrate.

The thicknesses  $t_1$ ,  $t_2$ ,  $t_3$ , and  $t_4$  of the circuit lines (and associated pads) in FIGS. 1-8 should be in the range of about 3 microns to about 50 microns, as discussed in the "Related Art" section.

While FIGS. 1-8 illustrate thickness-varying circuit lines (and associated pads) on both the top surface 18 and the bottom surface 19 of the substrate 10, the present invention includes embodiments having thickness-varying circuit lines on either the top surface 18 or the bottom surface 19, but not on both surfaces.

FIGS. 9-12 illustrate preferred electronic structures that could be formed by the method described *supra* and illustrated in FIGS. 1-8. FIG. 9 illustrates a top view of a first electrical structure 80, in accordance with a first preferred structural embodiment of the present invention. The first electrical structure 80 includes a substrate 90 which may represent a device such as a chip carrier. As stated in the "Related Art" section, a fine circuitization (including pads) has a thickness between about 3 microns and about 10 microns, a medium circuitization (including pads) has a thickness between about 10 microns and about 17 microns, and a thick circuitization (including pads) has a thickness between about 17 microns and about 50 microns. In FIG. 9, circuit line 92 has a fine circuitization, circuit lines 94 and 100 each have a medium circuitization, and circuit lines 96 and 104 each have a thick circuitization. Note that the relative thicknesses of circuit lines 92, 94, 96, 100, and 104

are not explicitly shown because FIG. 9 is a top view. FIG. 9 shows the thin circuit line 92<sup>14</sup> to be coupled the substrate 90, wherein the thin circuit line 92 is coupled to a medium circuit line 94, and wherein the medium circuit line 94<sup>3,10</sup> is coupled to a thick circuit line 96. A thin pad 93, which is suitable for coupling with a wirebond interconnect such as a gold wire, is positioned at an end of the thin circuit line 92. The wirebond interconnect may be used to electrically couple the thin pad 93 to an electronic assembly such as a chip. A thick pad 98, which is suitable for coupling with a large solder ball such as a BGA solder ball, is positioned at an end of the thick circuit line 96. The large solder ball may be used to electrically couple the thick pad 98 to an electronic carrier such as a circuit card. FIG. 9 also shows a medium circuit line 100 coupled to the substrate 90, wherein the medium circuit line 100 is coupled to a thick circuit line 104. A medium pad 102, which is suitable for coupling with a small solder ball, is positioned within the medium circuit line 100. The small solder ball may be used to electrically couple the medium pad 102 to an electronic assembly, such as a chip, by any suitable method such as controlled collapse chip connection (C4). A thick pad 106, which is suitable for coupling with a large solder ball such as a BGA

solder ball, is positioned within the thick circuit line 104.

FIG. 10 illustrates a front cross-sectional view of a second electrical structure 200, in accordance with a second preferred structural embodiment of the present invention. The second electrical structure 200 includes a substrate 204 which may represent a device such as a chip carrier. In FIG. 10, an electronic assembly 240 (e.g., a chip) within an cavity 207 in a substrate 204 is coupled to the substrate 204 by use of an adhesive interface 242. A first circuit line 210 is coupled to a bottom surface 206 of the substrate 204, and is conductively coupled to the electronic assembly 240 by use of a wirebond interconnect 244. The wirebond interconnect 244 couples the electronic assembly 240 to an open surface 216 of a metallic coating 211. The metallic coating 211 is on a portion 217 of the bottom surface 218 of the first circuit line 210. The metallic coating 211 includes a first metal coating 212 on the bottom surface 218, and a second metal coating 214 on the first metal coating 212. The first circuit line 210 has a thickness  $t_s$ , which may be any thickness in the range of about 3 microns to about 50 microns, preferably in a range of about 3 microns to about 10 microns. As an example, the first circuit line 210 may include copper, the first metal coating 212 may include nickel, the

second metal coating 214 may include gold, and the wirebond interconnect 244 may include a gold wire. The "pad" to which the wirebond interconnect 244 is attached includes the volumetric portion 209 of the first circuit line 210 that is beneath the metallic coating 211. A second circuit line 220 is coupled to the bottom surface 206 of the substrate 204, and is conductively coupled to the first circuit line 210. The second circuit line 220 has a thickness  $t_6$  which may be any thickness in a range of about 3 microns to about 50 microns, other than  $t_5$ . While  $t_6$  is shown in FIG. 10 as exceeding  $t_5$ ,  $t_6$  may nevertheless be less than  $t_5$ . A third circuit line 230, of thickness  $t_7$ , where  $t_7 \neq t_6$  and  $t_7 > t_5$ , is coupled to the bottom surface 206 of the substrate 204 and is conductively coupled to the second circuit line 220. The third circuit line 230 includes a pad 232 which is coupled to a solder ball 250, wherein the pad 232 includes the volumetric portion of the third circuit line 230 that interfaces with the solder ball 250. If the solder ball 250 is a BGA solder ball connected to an electronic device 260 such as an electronic carrier (e.g., circuit card), where the BGA solder ball has a diameter in a range of about 25 mils to about 30 mils, then  $t_7$  should be in the range of about 17 microns to about 50 microns. If the solder ball 250 is a small solder ball connected to an

electronic device 260 such as an electronic assembly (e.g., chip), where the small solder ball has a diameter of about an order of magnitude less than the diameter of a BGA solder ball (i.e, about 2 to about 3 mils), then  $t_7$  should be in a range of about 10 microns to about 50 microns, preferably in a range of about 10 microns to about 17 microns.

37 FIG. 11 illustrates a front cross-sectional view of a third electrical structure 300, in accordance with a third preferred structural embodiment of the present invention. The third electrical structure 300 includes a substrate 304 which may represent a device such as a chip carrier. In FIG. 11, an electronic assembly 340 (e.g., a chip) on a top surface 305 of a substrate 304 is coupled to the substrate 304 by use of an adhesive interface 342. A first circuit line 310 is coupled to the top surface 305 of the substrate 304, and is conductively coupled to the electronic assembly 340 by use of a wirebond interconnect 344. The wirebond interconnect 344 couples the electronic assembly 340 to an open surface 316 of a metallic coating 311. The metallic coating 311 is on a portion 317 of the top surface 318 of the first circuit line 310. The metallic coating 311 includes a first metal coating 312 on the top surface 318 of the first circuit line 310, and a second metal coating 314

on the first metal coating 312. The first circuit line 310 has a thickness  $t_8$ , which may be any thickness in the range of about 3 microns to about 50 microns, preferably in a range of about 3 microns to about 10 microns. The first circuit line 310 and the metallic coating 311 may include the same materials as stated *supra* in the example for the first circuit line 210 and metallic coating 211 in FIG. 10. The "pad" to which the wirebond interconnect 344 is attached includes the volumetric portion 309 of the first circuit line 310 that is beneath the metallic coating 311. A second circuit line 320, of thickness  $t_9$ , where  $t_9$  is unequal to  $t_8$  and preferably greater than  $t_8$ , is coupled to the bottom surface 306 of the substrate 304, and is conductively coupled to the first circuit line 310 by a PTH 308. The second circuit line 320 includes a pad 332 which is coupled to a solder ball 350, wherein the pad 332 includes the volumetric portion of the second circuit line 320 that interfaces with the solder ball 350. The solder ball 350 may be coupled to an electronic device 360 such as an electronic carrier (e.g., circuit card) or an electronic assembly (e.g., chip). Ranges of values for the thickness  $t_9$  and the solder ball 350 diameter are based on the same considerations as are the ranges of values for thickness  $t_7$  and solder ball 250 diameter, respectively, as discussed *supra*

for FIG. 10.

67 FIG. 12 illustrates a front cross-sectional view of a fourth electrical structure 400, in accordance with a fourth preferred structural embodiment of the present invention. The fourth electrical structure 400 includes a substrate 404 which may represent a device such as a chip carrier. In FIG. 12, a first circuit line 410 is coupled to a top surface 405 of a substrate 404. An electronic assembly 440 (e.g., a chip) is conductively coupled to the first circuit line 410 by use of an interfacing small solder ball 442 such as a C4 solder ball having a diameter between about 2 mils and about 3 mils. The first circuit line 410 has a thickness  $t_{10}$  which may be any thickness in the range of about 10 microns to about 50 microns, preferably in a range of about 10 microns to about 17 microns. The "pad" to which the small solder ball 442 is attached includes the volumetric portion 409 of the first circuit line 410 that is beneath the small solder ball 442. A second circuit line 420, of thickness  $t_{11}$  where  $t_{11}$  is unequal to  $t_{10}$ , is coupled to the bottom surface 406 of the substrate 404, and is conductively coupled to the first circuit line 410 by a PTH 408. The second circuit line 420 includes a pad 432 which is coupled to a solder ball 450, wherein the pad 432 includes the volumetric portion of the second circuit

line 420 that interfaces with the solder ball 450. The solder ball 450 may be coupled to an electronic device 460 such as an electronic carrier (e.g., circuit card) or an electronic assembly (e.g., chip). Ranges of values for the thickness  $t_{11}$  and the solder ball 450 diameter are based on the same considerations as are the ranges of values for thickness  $t$ , and solder ball 250 diameter, respectively, as discussed *supra* for FIG. 10.

5 57 While preferred and particular embodiments of the present invention have been described herein for purposes of illustration, many modifications and changes will become apparent to those skilled in the art. Accordingly, the appended claims are intended to encompass all such modifications and changes as fall within the true spirit and scope of this invention.